

**Ultra-low Power 8-bit MCU: 1T8051, 32KB eFlash, 2KB + 256B SRAM, 12-bit ADC, CAN
 No Crystal/LDO/RC Circuit, Rich Interfaces, Anti-crash, Anti-copy**

Product Features

● Ultra-low power management system

- 1.1 μA @ 3.0 V DeepSleep mode + timed wakeup, running at low clock speed, data retention for IO, SRAM and register
- 0.75 μA @ 3.0 V Stop mode, clock source stop, data retention for IO, SRAM and register
- 80 $\mu\text{A}/\text{MHz}$ @ 3.0 V Active mode
- Built-in ROSC/LDO/POR, board-level system requires no crystal / LDO / reset circuit

● Core

- 8-bit high-performance 8051 MCU, 1T, 6–12 times faster than the regular 8051

● Memory

- RAM: 256 B Idata, 2 KB Xdata
- 32 KB eFlash / 1 KB EEPROM

● GPIO: up to 17 pcs, configurable pull up/down modes

● PWM: 11 \times 16-bit PWM outputs

● Timer/counter

- 3 \times 16-bit GTimers supporting complementary PWM output with dead-time insertion
- 1 \times 16-bit LPTimer with PWM output
- 1 \times WDT

● Clock

- Internal RCH: 24 MHz
- Internal RCL: 38 kHz
- External crystal oscillator: 24 MHz (max.)
- External clock input: 24 MHz (max.)

● Communication interface

- UART: UART0 / UART1 / UART2 / UART3
- CAN: 1x, CAN2.0 A/B
- I2C: master/slave, up to 400 kbps (max.)
- SPI: 1 channel, master/slave, Mode 0/1/2/3 protocol, up to 12 Mbps



TSSOP20 (6.5*4.4mm)

QFN20 (3*3mm)

● Beeper: with configurable output frequency / polarity

● Analog peripherals

- ADC: 8-channel 12-bit SAR ADC, 1 Msps sampling rate
- Low-voltage detection (LVD), monitoring supply voltage
- Low-voltage reset (LVR), anti-crash

● Security

- Hardware-level anti-copy board
- 16-byte UUID

● Electrical characteristics

- Operating voltage: 2.5–5.5 V
- Operating temperature:
 - 40°C–105°C (\leq 16 MHz)
 - 40–85°C (24MHz)
- ESD: 8 kV (HBM)

● Development support

- Bootloader, supporting download via UART & updating of ISP and IAP programs
- Complete SDK and EVB HDK
- Offline programmer and UMP tool

● Selection table

Type	Model
32 KB	UM8006-ACTE (TSSOP20)
	UM8006-ACQE (QFN20)

1 Overview

UM8006 is a low-power 8-bit IoT chip with a wide operating voltage of 2.5–5.5 V, which is developed by Unicmicro based on single-cycle 8051 core. Adopting a unique low-power design technology, the chip integrates 32 KB Flash, SRAM (2 KB + 256 B), 12-bit SAR ADC (1 Msps), as well as universal peripheral communication interfaces such as UART, SPI, I2C, PWM and so on.

With built-in high-speed ROSC, LDO and POR, and no crystal/LDO/reset circuit required for the board-level system, UM8006 is featured by high integration of resources, high interference immunity, high reliability, low power consumption and minimal peripheral components. It also supports Keil MDK, C language and assembly language for software development.

Applications:

- Industrial IoT terminals
- Smart city, smart home, etc.
- Intelligent sensor terminal applications
- General controller applications such as toy control

2 Functional Block Diagram

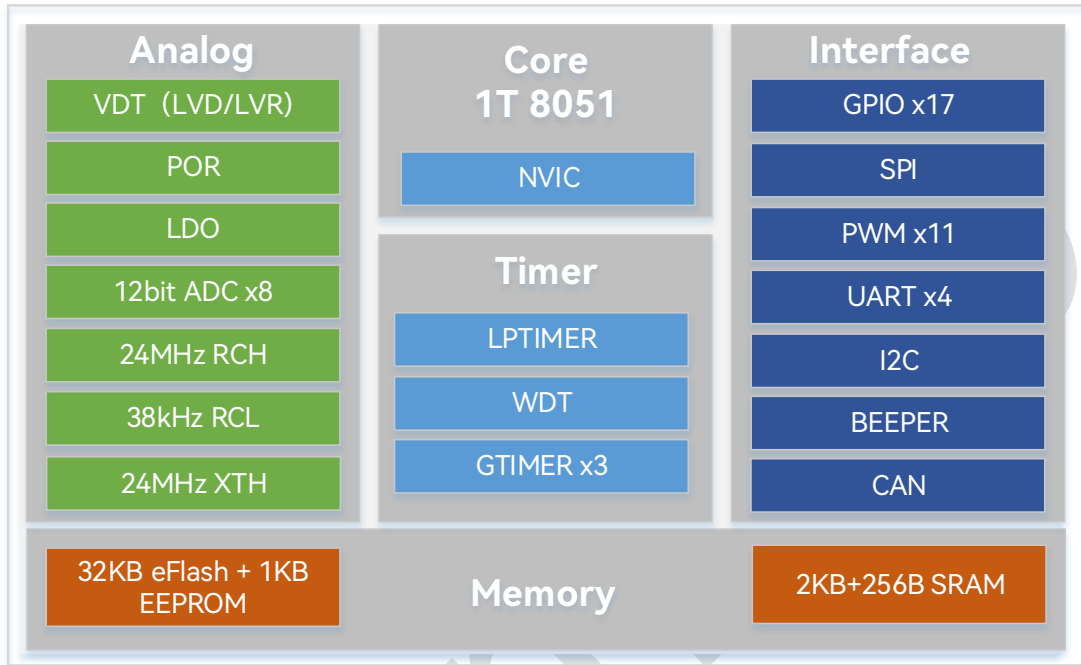


Figure 2-1: Functional Block Diagram

3 Package and Pin Description

3.1 Pinout Diagram

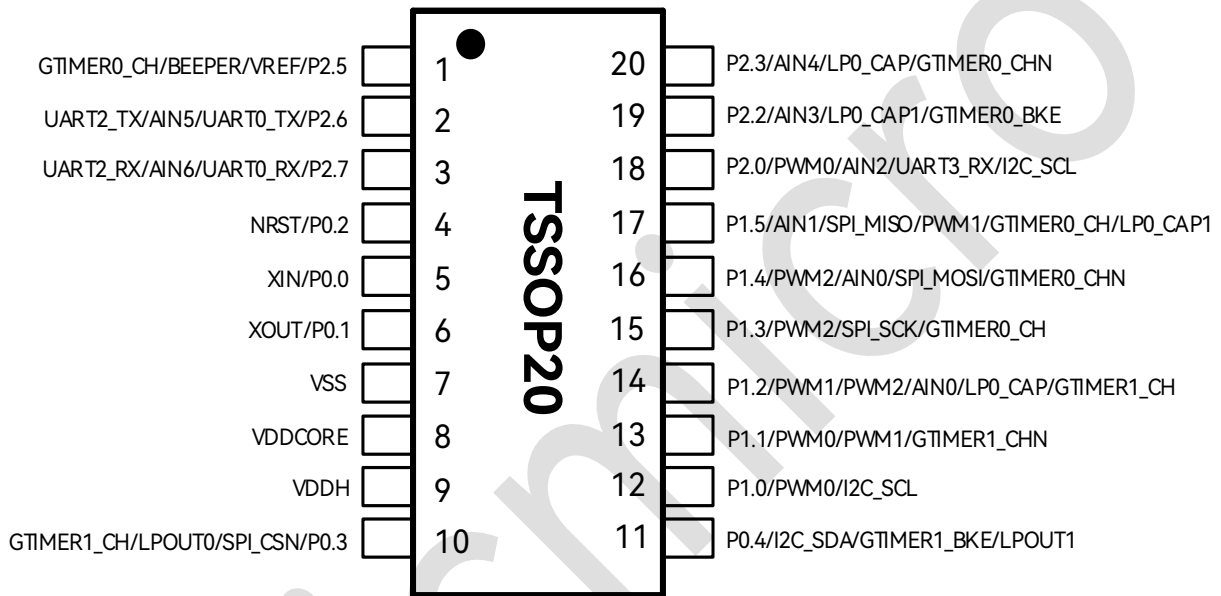


Figure 3-1: TSSOP20 Pinout Diagram

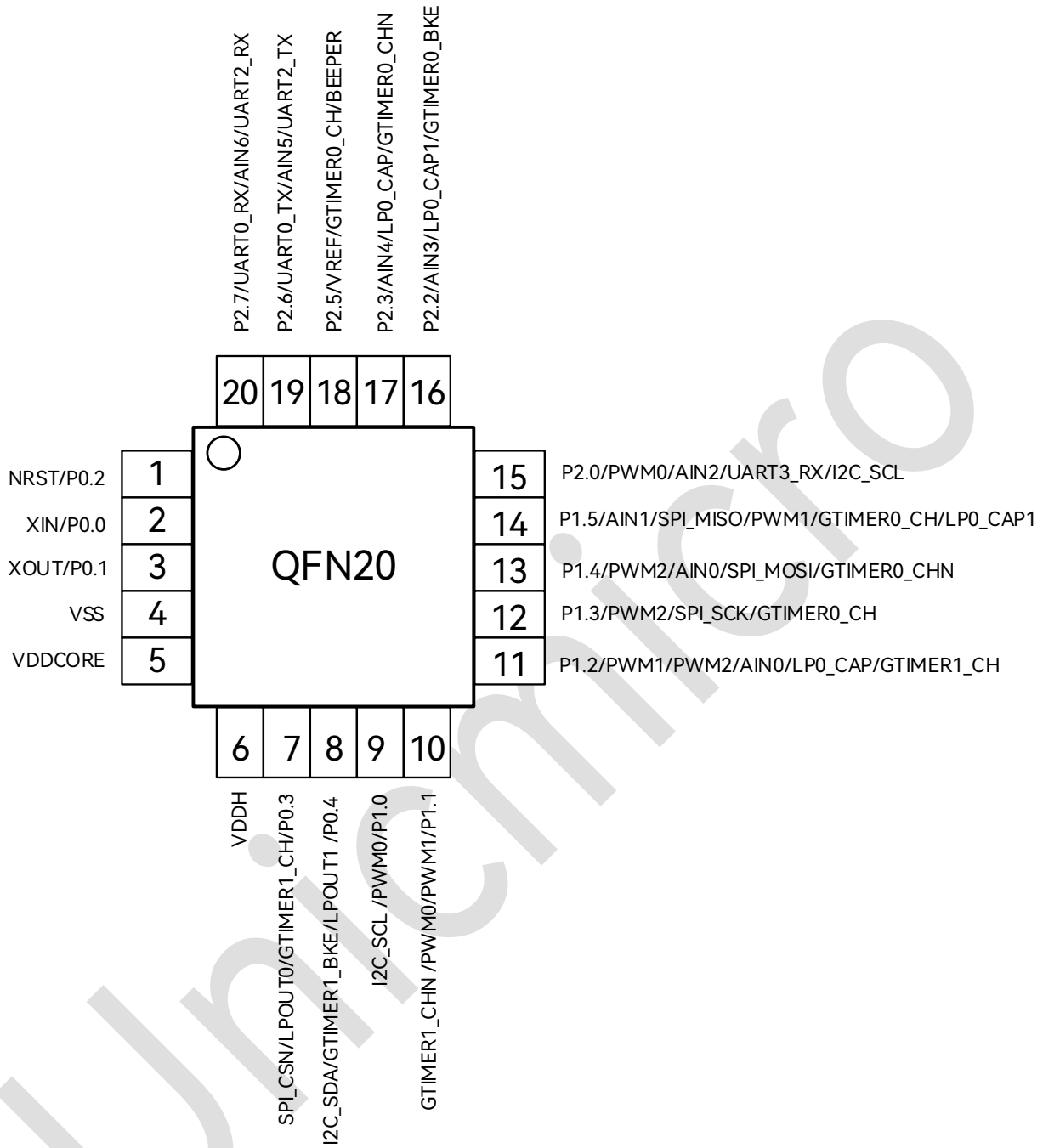


Figure 3-2: QFN20 Pinout Diagram

3.2 Alternate Function

Table 3-1: Pin Alternate Function

Pin No.		Config	Pxx_CFG[2:0]								
TSSOP20	QFN20		0	1	2	3	4	5	6	7	
1	18	VREF	P2.5	UART3_TX	SPI_CSN	I2C_SCL	GTIMER0_CH	GTIMER0_BKE	BEEPER	UART0_RX	
2	19	AIN5	P2.6	UART0_TX	UART2_TX	SPI_MISO	LPOUT1	GTIMER1_CH	GTIMER2_CH	-	
3	20	AIN6	P2.7	UART0_RX	UART2_RX	SPI_MOSI	I2C_SCL	GTIMER1_CHN	GTIMER2_BKE	BEEPER	
4	1	NRST/P0.2	-	-	-	-	-	-	-	-	
5	2	XIN	P0.0	UART2_RX	SPI_CSN	LPOUT0	GTIMER1_CHN	GTIMER2_BKE	CAN_TX	-	
6	3	XOUT	P0.1	UART2_TX	SPI_SCK	I2C_SDA	LPOUT1	GTIMER0_BKE	GTIMER2_CHN	CAN_RX	
7	4	VSS	-	-	-	-	-	-	-	-	
8	5	VDDCORE	-	-	-	-	-	-	-	-	
9	6	VDDH	-	-	-	-	-	-	-	-	
10	7	LPT_OUT	P0.3	CLKOUT	UART2_TX	UART3_RX	SPI_CSN	LPOUT0	GTIMER1_CH	CAN_TX	
11	8	-	P0.4	UART2_RX	SPI_SCK	I2C_SDA	LPOUT1	GTIMER1_BKE	GTIMER2_CHN	CAN_RX	
12	9	-	P1.0	UART1_RX	UART2_TX	PWM0	I2C_SCL	LP0_IN	GTIMER2_CH	-	
13	10	-	P1.1	UART1_TX	UART3_RX	PWM1	SPI_MISO	LP0_TRG	GTIMER1_CHN	PWM0	
14	11	AIN0	P1.2	UART0_RX	UART3_TX	PWM2	LP0_CAP	GTIMER1_CH	PWM1	CAN_TX	
15	12	-	P1.3	UART0_TX	UART2_RX	SPI_SCK	I2C_SDA	LP0_IN	GTIMER0_CH	PWM2	
16	13	AIN0	P1.4	UART1_RX	PWM2	SPI_MOSI	LP0_TRG	GTIMER0_CHN	GTIMER1_BKE	CAN_RX	
17	14	AIN1	P1.5	UART1_TX	PWM1	SPI_MISO	GTIMER0_CH	GTIMER1_BKE	GTIMER2_CH	LP0_CAP1	
18	15	AIN2	P2.0	UART3_RX	PWM0	SPI_MOSI	I2C_SCL	LPOUT0	GTIMER0_CHN	-	
19	16	AIN3	P2.2	UART3_TX	SPI_CSN	SPI_MISO	I2C_SDA	GTIMER0_BKE	GTIMER2_CHN	LP0_CAP1	
20	17	AIN4	P2.3	UART3_RX	SPI_SCK	SPI_MOSI	LP0_CAP	GTIMER0_CHN	GTIMER2_BKE	CAN_RX	

3.3 Pin Description

Table 3-2: Pin Description

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
1	18	P2.5	I/O	DI	-	P2.5 (default)	General-purpose digital input/output pin
						BEEPER	Beeper output signal
						VREF	V _{REF} input of ADC
						UART0_RX	RX signal of UART0
						UART3_TX	TX signal of UART3
						SPI_CSN	CS signal of SPI
						I2C_SCL	SCL signal of I2C
						GTIMER0_CH	Capture and PWM signals of GTimer0
						GTIMER0_BKE	Break signal of GTimer0
2	19	P2.6	I/O	DI	-	P2.6 (default)	General-purpose digital input/output pin
						UART0_TX	TX signal of UART0
						AIN5	CH5 signal of ADC
						UART2_TX	TX signal of UART2 (for download via BOOT UART, and shall be used with NRST signal.)
						SPI_MISO	MISO signal of SPI
						LPOUT1	PWM1 signal of LPTimer
						GTIMER1_CH	Capture and PWM signals of GTimer1
						GTIMER2_CH	Capture and PWM signals of GTimer2
3	20	P2.7	I/O	DI	-	P2.7 (default)	General-purpose digital input/output pin
						UART0_RX	RX signal of UART0
						AIN6	CH6 signal of ADC

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						UART2_RX	RX signal of UART2 (for download via BOOT UART, and shall be used with NRST signal.)
						SPI_MOSI	MOSI signal of SPI
						I2C_SCL	SCL signal of I2C
						GTIMER1_CHN	PWM reverse signal of GTimer1
						GTIMER2_BKE	Break signal of GTimer2
						BEEPER	Beeper signal
4	1	P0.2	I/O	DI	PU	NRST (default)	Reset pin for low-level reset and internal forced pull-up. This signal is necessary for batch download via UART, it is recommended to access this pin signal (pad or pin) onto PCB.
						P0.2	General-purpose digital input/output pin
5	2	P0.0	I/O	DI	-	P0.0 (default)	General-purpose digital input/output pin
						XIN	Crystal oscillator input pin
						UART2_RX	RX signal of UART2
						SPI_CSN	CS signal of SPI
						LPOUT0	PWM0 signal of LPTimer
						GTIMER1_CHN	PWM reverse signal of GTimer1
						GTIMER2_BKE	Braking signal of GTimer2
CAN_TX	TX signal of CAN						
6	3	P0.1	I/O	DI	-	P0.1 (default)	General-purpose digital input/output pin
						XOUT	Crystal oscillator output pin
						UART2_TX	TX signal of UART2
						SPI_SCK	SCK signal of SPI
						I2C_SDA	SDA signal of I2C
						LPOUT1	PWM1 signal of LPTimer
GTIMER0_BKE	Break signal of GTimer						

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						GTIMER2_CHN	PWM reverse signal of GTimer2
						CAN_RX	RX signal of CAN
7	4	VSS	G	AP	-	VSS	Power ground
8	5	VDDCORE	P	AP	-	VDDCORE	2.5-V output of internal LDO (1- μ F capacitance is required)
9	6	VDDH	P	AP	-	VDDH	Chip supply 2.5–5.5 V
10	7	P0.3	I/O	DI	-	P0.3 (default)	General-purpose digital input/output pin
						LPT_OUT	Output signal of LPTimer
						CLKOUT	Output signal of clock
						UART2_TX	TX signal of UART2
						UART3_RX	RX signal of UART3
						SPI_CSN	CS signal of SPI
						LPOUT0	PWM0 signal of LPTimer
						GTIMER1_CH	Capture and PWM signals of GTimer1
11	8	P0.4	I/O	DI	-	P0.4 (default)	General-purpose digital input/output pin
						UART2_RX	RX signal of UART2
						SPI_SCK	SCK signal SPI
						I2C_SDA	SDA signal of I2C
						LPOUT1	PWM1 signal of LPTimer
						GTIMER1_BKE	Break signal of GTimer1
						GTIMER2_CHN	PWM reverse signal of GTimer2
CAN_RX	RX signal of CAN						
12	9	P1.0	I/O	DI	-	P1.0 (default)	General-purpose digital input/output pin
						PWM0	PWM0 signal
						LP0_IN	LPTimer input signal
						I2C_SCL	SCL signal of I2C
						UART1_RX	RX signal of UART1
						UART2_TX	TX signal of UART2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						GTIMER2_CH	Capture and PWM signals of GTimer2
13	10	P1.1	I/O	DI	-	P1.1 (default)	General-purpose digital input/output pin
						PWM0	PWM0 signal
						PWM1	PWM1 signal
						UART1_TX	TX signal of UART1
						UART3_RX	RX signal of UART3
						SPI_MISO	MISO signal of SPI
						LP0_TRG	Trigger signal of LPTimer0
						GTIMER1_CHN	PWM reverse signal of GTimer1
14	11	P1.2	I/O	DI	-	P1.2 (default)	General-purpose digital input/output pin
						PWM2	PWM2 signal
						AIN0	CH0 signal of ADC
						PWM1	PWM1 signal
						UART0_RX	RX signal of UART0
						UART3_TX	TX signal of UART3
						LP0_CAP	Capture signal of LPTimer0
						GTIMER1_CH	Capture and PWM signals of GTimer1
15	12	P1.3	I/O	DI	-	P1.3 (default)	General-purpose digital input/output pin
						UART0_TX	TX signal of UART0
						PWM2	PWM2 signal
						UART2_RX	RX signal of UART2
						SPI_SCK	SCK signal SPI
						I2C_SDA	SDA signal of I2C
						LP0_IN	LPTimer input signal
						GTIMERO_CH	Capture and PWM signals of GTimer0

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
16	13	P1.4	I/O	DI	-	P1.4 (default)	General-purpose digital input/output pin
						UART1_RX	RX signal of UART1
						AIN0	CH0 signal of ADC
						SPI_MOSI	MOSI signal of SPI
						PWM2	PWM2 signal
						LP0_TRG	Trigger signal of LPTimer0
						GTIMER0_CHN	PWM reverse signal of GTimer0
						GTIMER1_BKE	Braking signal of GTimer1
17	14	P1.5	I/O	DI	-	P1.5 (default)	General-purpose digital input/output pin
						UART1_TX	TX signal of UART1
						SPI_MISO	MISO signal of SPI
						AIN1	CH1 signal of ADC
						PWM1	PWM1 signal
						GTIMER0_CH	Capture and PWM signals of GTimer0
						GTIMER1_BKE	Braking signal of GTimer1
						GTIMER2_CH	Capture and PWM signals of GTimer2
18	15	P2.0	I/O	DI	-	P2.0 (default)	General-purpose digital input/output pin
						AIN2	CH2 signal of ADC
						UART3_RX	RX signal of UART3
						PWM0	PWM0 signal
						SPI_MOSI	MOSI signal of SPI
						I2C_SCL	I2C_SCL
						LPOUT0	PWM0 signal of LPTimer
GTIMER0_CHN	PWM reverse signal of GTimer0						
19	16	P2.2	I/O	DI	-	P2.2 (default)	General-purpose digital input/output pin

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						AIN3	CH3 signal of ADC
						UART3_TX	TX signal of UART3
						SPI_CSN	CS signal of SPI
						SPI_MISO	MISO signal of SPI
						I2C_SDA	SDA signal of I2C
						GTIMER0_BKE	Break signal of GTimer0
						GTIMER2_CHN	PWM reverse signal of GTimer2
						LP0_CAP1	Capture1 signal of LPTimer
20	17	P2.3	I/O	DI	-	P2.3 (default)	General-purpose digital input/output pin
						AIN4	CH4 signal of ADC
						UART3_RX	RX signal of UART3
						SPI_SCK	SCK signal SPI
						SPI_MOSI	MOSI signal of SPI
						LP0_CAP	Capture signal of LPTimer0
						GTIMER0_CHN	PWM reverse signal of GTimer0
						GTIMER2_BKE	Break signal of GTimer2
						CAN_RX	RX signal of CAN

Notes:

A—analog signal; D—digital signal; I—input; O—output; G—ground; P—power; PU—pull up;

PD—pull down; HZ—high impedance state.

4 Electrical characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1: Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
V _{SS}	External supply voltage	-0.3	-	V
V _{DDH}		-	+6.0	V
T _{stg}	Storage temperature	-55	+150	°C
T _J	Junction temperature	-40	+125	°C
I _{DD}	Max. input current of V _{DDH} pin	-	50	mA
I _{SS}	Max. output current of V _{SS} pin	-	50	mA
V _{ESD(HBM)}	ESD protection voltage	-8	+8	kV

Note: The input voltage of IO pin shall not exceed VDDH, otherwise the chip will be damaged.

4.2 Operating Condition

4.2.1 General Operating Condition

Table 4-2: General Operating Condition

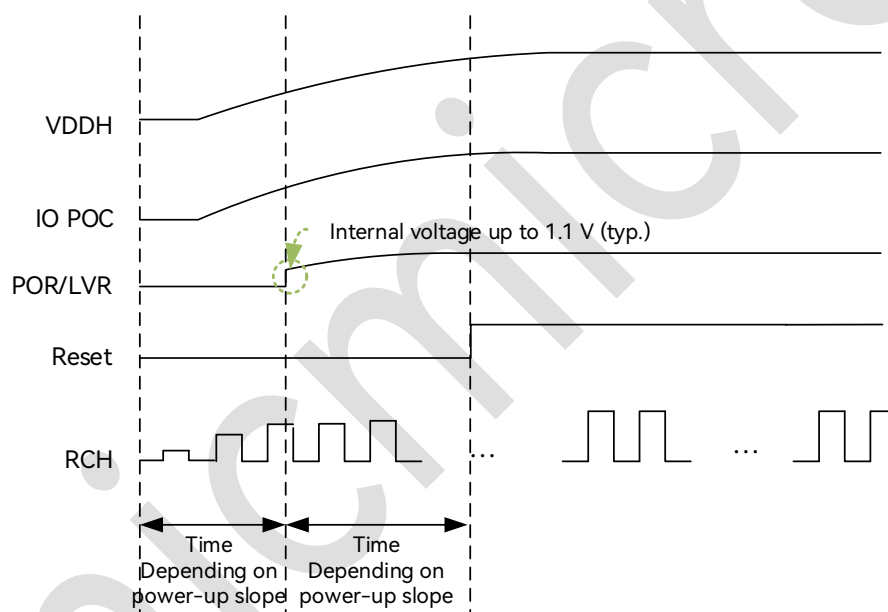
Symbol	Description	Min.	Max.	Unit	
V _{DDH}	Operating voltage	2.5	5.5	V	
T _A	Ambient temperature	F _{sys} = 24 MHz	-40	+85	°C
		F _{sys} ≤ 16 MHz	-40	+105	°C
F _{sys}	System frequency	0.1	24	MHz	

Note: When F_{sys} is lower than 2 MHz, Flash can only fetch and execute code, but cannot erase or write.

4.2.2 Operating Condition at Power-up / Power-down

Table 4-3: Operating Condition at Power-up / Power-down

Symbol	Description	Min.	Max.	Unit
t_{VDDH}	V_{DDH} rise time rate	0	110000	$\mu\text{s}/\text{V}$
	V_{DDH} fall time rate	0	110000	



Note: In the case of low-voltage reset occurs during power-down, the whole power-up process shall be experienced after powering up again.

4.2.3 VDT Voltage Detection (LVR/LVD)

Unless otherwise specified, $V_{DDH} = 3.3 \text{ V}$, $T_A = -40\text{--}105^\circ\text{C}$.

Table 4-4: Low Voltage Detection (LVR) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVR}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVR}	Detection threshold	Deepsleep mode	-	0.9	-	V
		Active mode	-	1.1	-	V
V_{HYS}	Hysteresis voltage	-	-	100	-	mV

Table 4-5: Low Voltage Detection (LVD) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVD}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVD}	Detection threshold	ADJ_LVD<3:1>=000 ADJ_LVD<3:1>=001 ADJ_LVD<3:1>=010 ADJ_LVD<3:1>=011 ADJ_LVD<3:1>=100 ADJ_LVD<3:1>=101 ADJ_LVD<3:1>=110 ADJ_LVD<3:1>=111	-	4.39 3.95 3.59 3.29 3.04 2.82 2.63 2.46	-	V
V_{HYS}	Hysteresis voltage	-	-	100	-	mV
I_{VDD}	Current consumption	-	-	800	-	nA

4.2.4 Operating Current Characteristics

Current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, flip speed of I/O pin, location of program in memory, code executed, etc.

Table 4-6: Operating Current Characteristics

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit	
I_{DD}	Operating current	Active mode: $V_{DDH} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$; all peripherals are disabled, the code runs “while(1){}” in Flash. CCLK = 16 MHz	-	1.28	-	mA	
		Active mode: $V_{DDH} = 3.3\text{ V}/5$, $T_A = 25\text{ }^\circ\text{C}$; all peripherals are enabled, the code runs “while(1){}” in Flash.	CCLK = 16 MHz	-	1.5	-	mA
			CCLK = 4 MHz	-	0.5	-	mA
			CCLK = 2 MHz	-	0.3	-	mA
		Sleep mode: $V_{DDH} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$	-	0.24	-	mA	
		DeepSleep mode: $V_{DDH} = 3.3\text{ V}$; $T_A = 25\text{ }^\circ\text{C}$	-	1.1	-	μA	
Stop mode: $V_{DDH} = 3.3\text{ V}$; $T_A = 25\text{ }^\circ\text{C}$	-	0.75	-	μA			

Note: The typical value is not guaranteed. The values in the list are obtained at normal voltage and room temperature.

4.2.5 Wakeup Time from Low-power Mode

Table 4-7: Wakeup Time from Low-power Mode

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{wakeup}	DeepSleep mode to Active mode	Regulator voltage = 2.5 V, $T_A = 25^\circ\text{C}$, 16MHz	-	16.6	-	μs

4.2.6 Internal Clock Source Characteristics

➤ Internal RCH oscillator

Unless otherwise specified, $V_{\text{DDH}} = 3.3 \text{ V}$, $T_A = -40\text{--}105^\circ\text{C}$.

Table 4-8: RCH Oscillator Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Clock frequency	$T_A = -40^\circ\text{C}\text{--}105^\circ\text{C}$	$24 * (1 - 2.5\%)$	24	$24 * (1 + 2.5\%)$	MHz
Duty	Duty cycle	$F_{\text{HSI}} = 24 \text{ MHz}$	45	50	55	%
t_{SU}	Clock settling time	-	-	1.2	-	μs
I_{VDD}	Current consumption	-	-	80	-	μA

➤ Internal RCL oscillator

Unless otherwise specified, $V_{\text{DDH}} = 3.3 \text{ V}$, $T_A = -40\text{--}105^\circ\text{C}$.

Table 4-9: RCL Oscillator Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Clock frequency	After trimming	$38 * (1 - 5\%)$	38	$38 * (1 + 5\%)$	kHz
Duty	Duty cycle	-	48	50	52	%
t_{SU}	Clock settling time	-	-	100	200	μs
I_{VDD}	Current consumption	-	-	260	-	nA

4.2.7 External Crystal Oscillator XTH Characteristics

Unless otherwise specified, $V_{\text{DDH}} = 3.3 \text{ V}$, $T_A = -40\text{--}105^\circ\text{C}$.

Table 4-10: XTH Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$F_{\text{OSC_IN}}$	Frequency range	-	2.0	16	24	MHz

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{SU}	Clock settling time	-	-	2	-	ms
I_{VDD}	Current consumption	-	-	0.9	-	mA
I_{lk}	Leakage current	-	-	0.01	-	μ A

4.2.8 Memory Characteristics

Table 4-11: eFlash Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ECflash	Sector endurance	-	20 K	-	-	cycle
RETflash	Data retention	-	10	-	-	year
t_{prog}	Word program time	-	-	-	20	μ s
t_{erase}	Sector erase time	-	2	-	5	ms
	Chip erase time	-	20	-	40	ms

4.2.9 IO Characteristics

Table 4-12: IO Characteristics

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{IL}	Logic low level input current	$V_I = 0$ V	-1	-	-	μ A
I_{IH}	Logic high level input current	$V_I = V_{DDH}$	-	-	+1	μ A
V_O	Output voltage	Output pin being active	0	-	V_{DD}	V
V_{IH}	Logic high level input voltage	-	$0.7 * V_{DDH}$	-	-	V
V_{IL}	Logic low level input voltage	-	-	-	$0.3 * V_{DDH}$	V
V_{hys}	Hysteresis voltage	-	$0.1 * V_{DDH}$	-	-	V
V_{OH}	Logic high level output voltage	5 V, output $I_{Load} = 16$ mA in high-drive mode output $I_{Load} = 8$ mA in low-drive mode	$V_{DDH} - 0.8$	-	-	V

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
		3.3 V, output $I_{Load} = 8$ mA in high-drive mode output $I_{Load} = 4$ mA in low-drive mode	2.4	-	-	V
V_{OL}	Logic low level output voltage	5 V, output $I_{Load} = 16$ mA in high-drive mode output $I_{Load} = 8$ mA in low-drive mode	-	-	0.5	V
		3.3 V, output $I_{Load} = 8$ mA in high-drive mode output $I_{Load} = 4$ mA in low-drive mode	-	-	0.4	V
I_{OH}	Logic high level output current	5 V, output in high-drive mode output in low-drive mode	- -	16 8	- -	mA
		3.3 V, output in high-drive mode output normally in low-drive mode	- -	8 4	- -	mA
I_{OL}	Logic low level output current	5 V, output in high-drive mode output in low-drive mode	- -	16 8	- -	mA
		3.3 V, output in high-drive mode output in low-drive mode	- -	8 4	- -	mA
R_{pup} R_{pdn}	Pull up / down current	5 V / 3.3 V	20	-	100	K Ω
C_{IN}	Input capacitance	5 V / 3.3 V	-	-	10	pF

4.2.10 ESD/Latchup Characteristics

All the data below are measured at $T_A = +25^\circ\text{C}$ based on ESDA/JEDEC standard.

Table 4-13: ESD/Latchup Characteristics

Symbol	Description	Class	Max.	Unit
$V_{\text{ESD(HBM)}}$	ESD @ Human Body Model	Class 3B	8000	V
$V_{\text{ESD(CDM)}}$	ESD @ Charge Device Model	Class C2	500	V
$V_{\text{ESD(MM)}}$	ESD @ Machine Model	Class B	200	V
I_{latchup}	Latch up current	Class IA	200	mA

4.2.11 ADC Characteristics

The following electrical characteristics are measured at $T_A = 25^\circ\text{C}$, $V_{\text{DDA}} = 3.3\text{ V}$ and $V_{\text{DDD25}} = 2.5\text{ V}$.

Table 4-14: ADC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{ADCIN}	Input voltage range	Single ended	0	-	V_{DD}	V
V_{REF}	ADC reference voltage	-	-	V_{DD}	-	V
I_{ADC}	-	-	0.7	0.9	1.2	mA
C_{ADCIN}	ADC input capacitance	-	3.5	4	4.5	pF
F_{ADCCLK}	ADC clock frequency	-	0.5	4	16	MHz
t_{ADCSTART}	Startup time of ADC bias current	-	2	3	4	μs
t_{ADCCONV}	Conversion time	-	16	16	20	cycle
ENOB	-	-	9.5	10	10.4	bit
DNL	Differential non-linearity	-	-2	± 1	2	LSB
INL	Integral non-linearity	-	-3	± 1	3	LSB
E_o	Offset error	-	-2	± 1	2	LSB
E_g	Gain error	-	-2	± 1	2	LSB

Note: Not tested in production.

5 Package Outline

5.1 QFN20 (3 * 3 mm)

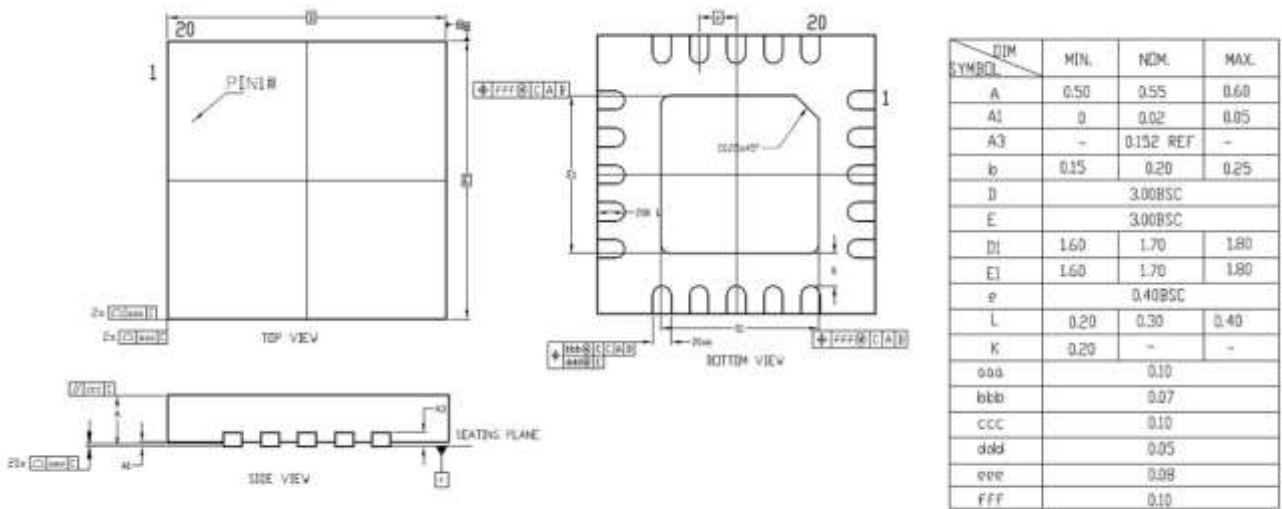


Figure 5-1: QFN20 Package Outline Drawing

5.2 TSSOP20 (6.5 * 4.4 mm)

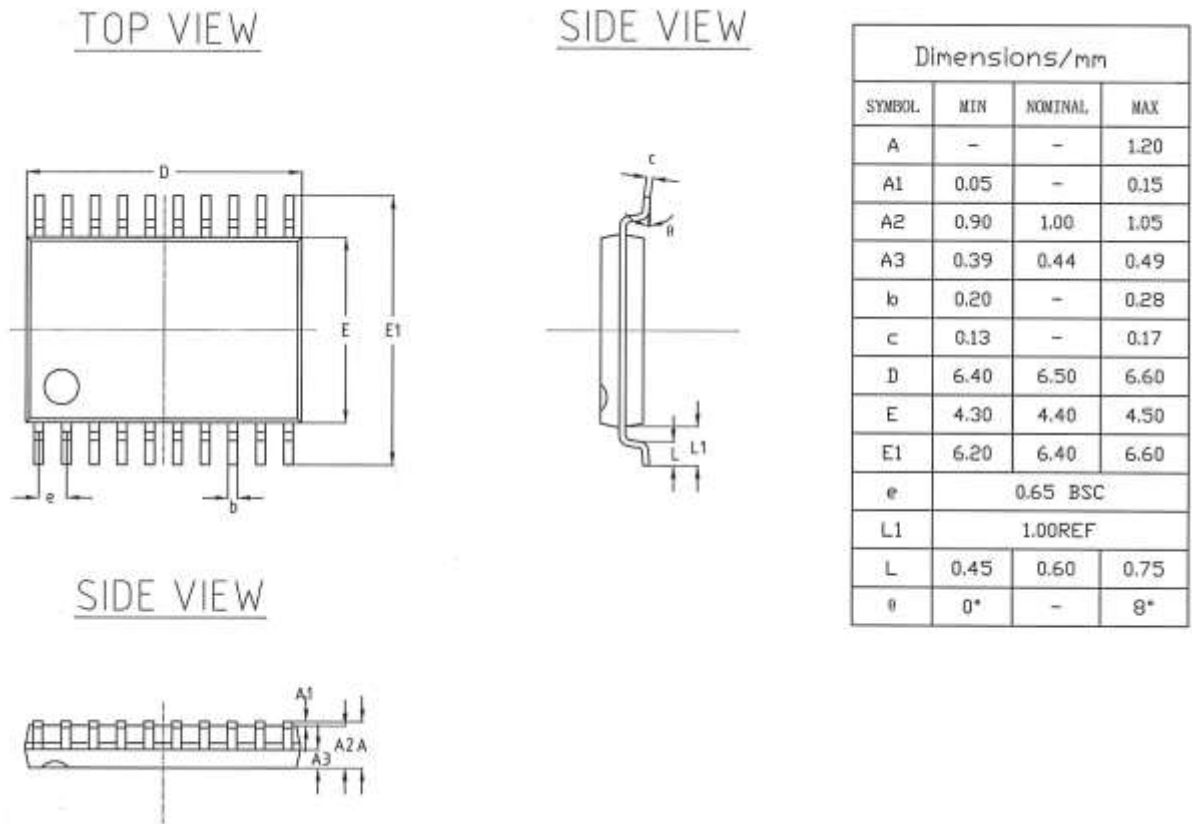


Figure 5-2: TSSOP20 Package Outline Drawing

6 Revision History

Version	Date	Description
V1.0	Jan-13-2022	Initial release.
V1.1	Feb-10-2022	<ol style="list-style-type: none"> Updated QFN20 package outline drawing. Updated pin descriptions. Updated TSSOP20 package outline drawing. Updated DC parameters. Deleted descriptions regarding T0/T1. Updated parameters of the internal RCL oscillator.
V1.2	Mar-11-2022	<ol style="list-style-type: none"> Modified the number of GTIMER into 3 and PWM into 11. Updated the functional block diagram. Added information regarding 1 KB EEPROM in the home page. Updated the pinout diagram. Added the chapter of <i>Alternate Function</i>. Updated pin descriptions. Updated parameters of the internal RCH oscillator.
V1.3	Mar-28-2022	<ol style="list-style-type: none"> Added the chapter of <i>Operating Condition at Power-up and Power-down</i>. Updated parameters of the internal RCH oscillator. Updated the operating temperature range.
V1.4	Apr-22-2022	<ol style="list-style-type: none"> Updated the SOP8 package outline drawing. Modified the value of 1.5 V into 2.5 V for the whole document. Updated the chapter of <i>Alternate Function</i> (modified the description for bit 7 of P13_CFG[2:0] into PWM2).
V1.5	Jul-13-2022	Adjusted the structures of home page and the chapter of <i>Electrical Characteristics</i> .
V1.6	Apr-18-2024	<ol style="list-style-type: none"> Deleted the information related to UM8006-ACSA (SOP8). Deleted the chapter of <i>IO Port Characteristics</i>. Updated the QFN20 package outline drawing.
V1.6.1	Jun-25-2024	<ol style="list-style-type: none"> Modified the remarks regarding UART0 and UART2 of P2.6 & P2.7 in the chapter of <i>Pin Description</i>. Replaced the fonts and adjusted formatting.
V1.6.2	Aug-26-2024	Updated the typical value of V_{LVD} in “Table 4-5: Low Voltage Detection (LVD) Characteristics”.

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